In recent years, product designs have changed rapidly. There is an increasing need for small, programmable, high performance products. Designers face greater demands for system reliability from consumers. Three of the more common circuits used to improve system reliability are Watchdog Timer, Low Voltage Reset and Power-On management. By combining these features, Intersil offers a small, powerful, cost effective solution for system designers. In addition, Intersil's X5000 series devices offer flexibility never before possible with resettable watchdog timeout periods, reprogrammable low voltage thresholds and various combinations of on-chip serial EEPROM.

Power On Reset Operation

The first, perhaps most critical safeguard that can be added to a system is a reliable power on reset. This circuit is designed to ensure that the microcontroller powers up correctly every time. The combination of power supply design and microcontroller sensitivity to power on conditions can make this difficult. Often, a noisy or slow power supply will cause the microcontroller to improperly initialize, resulting in system failure. One of the best ways to prevent this is to "hold" the microcontroller until the power supply stabilizes. This Power-On Reset feature is standard on all of Intersil's X5000 Series CPU Supervisors.

The Power-On Reset Circuit holds the RESET pin active (preventing the microcontroller from operating) until the Power supply voltage is above a fixed threshold for a nominal 250ms. The X51638 is a special family member. Its 800ms nominal power on reset period is ideal for devices with power supplies that have longer settling times on power up, for oscillators that take longer to stabilize or for systems that use FPGAs that must download code before they start their operation.

Low Voltage Reset Operation

The second most critical area to consider in preventing system failures is low voltage protection. In most systems, there are differing operating voltages for different components. As the power goes down, one or more devices may stop operating correctly. This is particularly bad if the failing device is the microcontroller. On the edge of operation, the microcontroller may execute incorrectly and send out incorrect data or turn on the wrong signal. Since other devices are likely still operating correctly, the system can fail. Sometimes the result is unexpected data changes in the memory. When activated, RESET remains active until the V_{CC} supply again exceeds the trip voltage for (a nominal) 250ms. This delay in releasing RESET helps to avoid frequent system reset conditions.

The Low Voltage Reset controller provided on Intersil's CPU supervisors protects systems from low voltage conditions by activating the RESET output when V_{CC} drops below a V_{CC} trip point. RESET is asserted until V_{CC} returns and stabilizes above the V_{CC} trip point. The V_{CC} trip points are factory set at one of several standard voltage levels. See Table 1

TABLE 1. FACTORY SET V_{trip} POINTS

POWER SUPPLY (V)	SUFFIX	MIN (V)	MAX (V)
4.5-5.5	-4.5A	4.5	4.75
4.5-5.5	Blank	4.25	4.50
2.7-5.5	-2.7A	2.85	3.0
2.7-5.5	-2.7	2.55	2.70
1.8-3.6	-1.8	1.7	1.8

Other V_{CC} trip points or tighter V_{CC} tolerances are possible by re-programming the low voltage trip point. This is a relatively simple process that is documented in each devices' data sheet. Intersil uniquely implements an "analog EEPROM" cell for setting the low voltage threshold. This requires very little current, can be reprogrammed thousands of times and remains stable over both time and temperature. Progamming the threshold requires the application of a 15V signal, so it is not something that will happen inadvertently.

To facilitate programming of the low voltage threshold, Intersil has a kit for programming small quantities of devices (XK5000). For high volume needs, standard component test/inspection equipment can be used. In the future, programming will be supported by standard EEPROM programmers. Look for future application notes that provide more detailed support documentation, For other information on reprogrammability or special options, please contact the factory.

Programmable Watchdog Timer

The low voltage and power-on reset circuits helps to keep a system operational. However, there are conditions that are impossible to predict. Many of these involve software or the hardware/software interface. For example:

- A software subroutine waiting for a peripheral to respond may never exit if the peripheral has failed.

- In a complicated design, many different programmers develop different pieces of code. Data passing is defined well, but not completely. When the unit is in the field, a condition arises that was not tested and unexpected data is passed, causing the software to "crash".

- Noise on an input causes the processor to enter an unexpected mode of operation.

To deal with these, and other potential system failures, more systems today incorporate a watchdog timer. A watchdog timer ensures system reliability by providing a RESET signal to the microcontroller, microprocessor, ASIC or DSP. This RESET signal returns the system to a known state, while the watchdog timer continues to monitor system operations, providing improved reliability.

Intersil's programmable watchdog timer provides several advantages over its competitors:

1. The designer can choose from three programmable time-out intervals. There is no need to decide on a factory preset time-out interval before prototypes begin.

2. The programmable watchdog timer can be disabled easily, via software, during debug or during field recalibration or upgrade. This eliminates the endless resets that normally occur during debug of a system with a fixed watchdog timer and it eliminates the need to remove hardware from the board to disable the watchdog.

3. Since software revisions may require a tighter or looser time-out interval, software programming of the time-out period results in easy system upgrades. This eliminates the need to make changes to the PC board, as is the case with hard-wired devices.

A watchdog timer is a simple countdown timer which activates a RESET signal when it reaches zero. This RESET signal provides the system reset for the microcontroller, microprocessor, ASIC or DSP. During normal operation, the system software sends a signal to reset the countdown timer to its maximum value before it reaches zero. If the system locks up or enters some unwanted state, or if the software operates unexpectedly or gets stuck in an infinite loop, the watchdog timer will time-out and assert the reset signal. By asserting the RESET, the system returns to a known state and continues to operate. After deasserting the RESET signal, the watchdog timer automatically begins another countdown, thus providing the system continuous reliability.

The system software provides the watchdog timer restart signal by toggling the Supervisory EEPROM $\overline{CS}$ pin HIGH to LOW. The watchdog timer begins to countdown from its maximum value once the $\overline{CS}$ is pulled low. If the $\overline{CS}$ remains low longer than the programmable time interval, the watchdog timer will 'time-out' and assert the reset signal. This edge triggered restart prevents the watchdog timer from being kept in a continuous restart mode without toggling $\overline{CS}$. This feature provides protection to the system even when restarting the watchdog timer.

Programming the Watchdog Timer

Two non-volatile bits (WD1, WD0) in the status register control the programmable watchdog timer intervals (See Table 2) These bits are accessed via a read/write status register command (as described in the data sheet.) As with any nonvolatile write operation, a write enable command preceeds the status register write operation. This write

enable command, which sets the WEL bit, helps prevent inadvertent changes to the watchdog timer intervals. In applications where the Watchdog timer setting is very critical, setting the WPEN bit to a '1' and soldering the $\overline{WP}$ pin active LOW creates a psuedo-OTP function that requires a both a hardware change and a series of software commands to change the watchdog time-out interval.

TABLE 2. STATUS RESGISTER EXAMPLE

7	6	5	4	3	2	1	0
WPEN	0	WD1	WD0	BP1	BP0	WEL	WIP

NOTE: Only available in devices with 16K, 32K, or 64K of EEPROM

The watchdog timer is programmable to four preset values: 200ms, 600ms, 1.4s and disabled, see Table 3 Disabling the watchdog timer provides for easy software debugging during prototyping without the nuisance of frequent resets. Once the watchdog timer is enabled (initially disabled from the factory) the watchdog timer will power-up and begin to count down once the power reset circuit (POR) has de-asserted the reset signal. Once enabled, Intersil's watchdog timer requires no initialization after power-up.

TABLE 3. WATCHDOG TIMER INTERVALS

WD1	WD0	MIN.	TYP	MAX	UNITS
1	0	100	200	300	ms
0	1	450	600	800	ms
0	0	1	1.4	2	sec
1	1	OFF			

Summary

Intersil's new family of supervisory EEPROMs combines Power-On Reset, Low Voltage Reset and Watchdog Timer features with standard SPI BlockLock™ EEPROM. Combined, these five features provide a small, powerful, cost efficient way to improve system reliability. Since it is not always necessary to use all three supervisory features or EEPROM, Intersil provides choices to give the designer the greatest possible flexibility. For a summary of the available devices, see Table 4.

TABLE 4. INTERSIL SUPERVISORY EEPROMS

INTERSIL DEVICE	LOW VOLTAGE RESET OPTIONS (V)	POWER ON RESET (ms)	WATCHDOG TIMER TIMEOUT PERIOD (s)	WATCHDOG TIMER RESET PERIOD (ms)	RESET ACTIVE LEVEL	EEPROM DENSITY
X5001	4.62 4.38 2.92 2.62 1.75	200	Off, .2, .6, 1.4	200	Low	0K
X5043/X5045		250		250	Low/High	4K
X5163/X5165						16K
X5323/X5325					Low/High	32K
X5643/X5645						64K
X51638		800	Off, .4, .6, 1.4	400		16K
X5168/X5169		250	N/A	N/A	Low/High	16K
X5328/X5329						32K
X5648/X5649						64K

For information regarding Intersil Corporation and its products, see www.intersil.com